REMARKS

Applicants concurrently file herewith an Excess Claim Fee Payment Letter, and a corresponding excess claim fee, for three (3) excess total claims.

Claims 1-25 are all of the claims presently pending in the application. Claims 1-22 have been merely editorially amended, and have not been substantively amended to more particularly define the invention. Claims 23-25 have been added to provide more varied protection for the claimed invention and to claim additional features of the invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicants specifically state that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1-3, 6-14, and 17-22 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Savas et al. (U.S. Patent No. 6,805,139) (hereinafter "Savas"). Claims 4, 5, 15 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Savas.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (e.g., as defined in exemplary claim 1) is directed to a method for manufacturing a semiconductor device. The method includes forming an SiOC-containing insulating film on a semiconductor substrate, selectively removing the insulating film and removing residue generated during selectively removing the insulating film with a fluoride-free alkaline stripper.

A conventional semiconductor device forming method may include forming a copper film on a semiconductor substrate, on which is then formed an SiOC film; forming a resist on the SiOC film and using the resist as a mask to form a hole by dry etching to expose a copper film surface; removing the resist by ashing; cleaning the inside of the hole with a stripper; and rinsing the product. During this process the side wall of the hole may be etched by the stripper during the cleaning step so that a desired shape cannot be formed.

The claimed invention of exemplary claim 1, on the other hand, provides a method for manufacturing a semiconductor device including removing residue generated during

selectively removing the insulating film with a fluoride-free weak alkaline stripper (e.g., see Application at page 3, lines 18-24). This allows the residue generated during selectively removing a low-dielectric-constant film made of, for example, SiOC, to be effectively removed without any problem or damage to the insulating film (see Application at page 3, lines 13-16).

II. THE PRIOR ART REFERENCE

The Examiner alleges that Savas teaches the claimed invention of claims 1-3, 6-14 and 17-22. Furthermore, the Examiner alleges that the claimed invention of claims 4, 5, 15 and 16 would have been obvious in view of Savas. Applicants submit, however, that there are elements of the claimed invention which are neither taught nor suggested by Savas.

That is, Savas does not teach or suggest "*removing residue generated during said selectively removing said insulating film with a fluoride-free weak alkaline stripper*" as recited in claim 1, and similarly recited in claims 2, 12 and 13.

Clearly, the novel features of the claimed invention are not taught or suggested by Savas. The Examiner attempts to rely on column 5, lines 1-10 and column 10, lines 11-15 of Savas to support her allegations. The Examiner, however, is clearly incorrect.

That is, nowhere, in these passages (nor anywhere else for that matter) does Savas teach or suggest a method for manufacturing a semiconductor device including removing residue generated during selectively removing the insulating film with a fluoride-free weak alkaline stripper. Indeed, Savas merely teaches removing residue generated during a high-dose ion-implementation process using a mixture of a principal active gas and an additive gas (see Savas at column 10, lines 2-17).

Savas teaches that in the case of a via etch and residue removal process, as is taught by the claimed invention, gases which contain fluorine, chlorine or bromine are used (see Savas at column 10, lines 12-14). Savas further teaches that additive gases including fluorine, chlorine or other halogens help in removing residues in the via cleaning stage (see Savas at column 10, lines 46-49). Savas does not even mention, let alone teach or suggest, using a fluoride-free weak alkaline stripper.

In contrast, the claimed invention, of exemplary claim 1, teaches using a fluoride-free weak alkaline stripper for removing residue generated during selectively removing a SiOC-

containing insulating film. Applicants have discovered that if the stripper contains fluoride ions, the insulating film may be often damaged. Furthermore, if the stripper is a strong alkaline or is acidic, it is difficult to effectively remove the residue without damage on the insulating film (see Application at page 5, lines 12-16).

Moreover, when the wafer is treated with a stripper containing ammonium fluoride, the modified layer of the semiconductor device is dissolved in the stripper. As a result, side etching of the SiOC film proceeds so that an interconnect trench having designed dimensions cannot be formed (see Application at page 14, lines 4-9).

This feature is clearly not taught or suggested by Savas.

Therefore, Applicants submit that there are elements of the claimed invention that are not taught or suggest by Savas. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. NEW CLAIMS

New claims 23-25 are added to provide more varied protection for the claimed invention and to claim additional features of the invention. These claims are independently patentable because of the novel features recited therein.

Applicants respectfully submit that new claims 23-25 are patentable over any combination of the applied references at least for the reasons to those set forth above with respect to claims 1-22.

IV. FORMAL MATTERS AND CONCLUSION

Applicants respectfully request the Examiner to acknowledge Applicants claim to foreign priority made on July 9, 2003 and the corresponding priority document filed therewith.

In view of the foregoing, Applicants submit that claims 1-25, all of the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: March 11, 2005

Scott M. Tulino, Esq.
Registration No. 48,317

Sean M. McGinn, Esq.
Registration No. 34,386

McGinn & Gibb, PLLC
Intellectual Property Law
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254